Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A phase difference detector adapted to generate a phase difference signal indicative of a phase difference between a first signal and a second signal, comprising:

a first bistable element clocked by the first signal and having an output terminal to provide a first output signal;

a second bistable element clocked by the second signal and having an output terminal to provide a second output signal;

means for determining a change of said phase difference signal, responsive to said first and second output signals;

a reset circuit having first and second input terminals respectively connected to receive said first and second output signals and adapted to determine a resetting of the first and the second bistable elements responsive to an attainment of a respective prescribed state of the first and the second output signals, said first and second input terminals of the reset circuit substantially symmetrical to each other from a point of view of a respective input impedance associated with each of them; and

a symmetrization element coupled to the output terminals of the first and second bistable elements, the symmetrization element including two transistors coupled in series and having control terminals coupled to the respective output terminals of the first and second bistable elements.

2. (Previously Presented) The phase difference detector of claim 1 wherein the reset circuit includes, associated with said first and second input terminals, input impedance symmetrization means that comprise part of the symmetrization element.

3. (Previously Presented) The phase difference detector of claim 2 wherein the reset circuit includes a logic circuit with a first logic input terminal and a second logic input terminal, respectively coupled to receive the first and the second signals and adapted to detect the attainment of the respective prescribed state by the first and the second output signals, and wherein said symmetrization means are associated with said first and second logic input terminals.

4. (Previously Presented) The phase difference detector of claim 3 wherein said symmetrization means include decoupling means of the first and second input terminals of the reset circuit from the first and second logic input terminals, respectively.

5. (Currently Amended) A phase-locked loop circuit adapted to generate an output signal locked in frequency and phase to a reference signal, comprising:

a phase difference detector adapted to detect a phase difference between the reference signal and a signal derived from the output signal, the phase difference detector including:

a first bistable element clocked by the reference signal and having an output terminal to provide a first output signal;

a second bistable element clocked by the derived signal and having an output terminal to provide a second output signal;

means responsive to said first and second output signals for determining a change of a phase difference signal that is indicative of a phase difference between the reference signal and the derived signal;

a reset circuit having first and second input terminals respectively connected to receive said first and second output signals and adapted to determine a resetting of the first and the second bistable elements responsive to an attainment of a respective prescribed state of the first and the second output signals, said first and second input terminals of the reset circuit substantially symmetrical to each other from a point of view of a respective input impedance associated with each of them; and

a symmetrization element coupled to the output terminals of the first and second bistable elements, the symmetrization element including two transistors coupled in series and having control terminals coupled to the respective output terminals of the first and second bistable elements; and

an oscillator controlled by the phase difference signal generated by the phase difference detector.

6. (Previously Presented) The phase-locked loop circuit of claim 5, further comprising a frequency divider adapted to generate the derived signal through division in frequency of the output signal of the phase-locked loop circuit, said divider being controlled to implement a division factor equal to an integer number.

7. (Previously Presented) The phase-locked loop circuit of claim 5, further comprising a frequency divider adapted to generate the derived signal through division in frequency of the output signal of the phase-locked loop circuit, said divider being controlled to implement an average division factor equal to a non-integer number.

8. (Currently Amended) A frequency synthesizer circuit, comprising:

a reference signal generator and a phase-locked loop circuitadapted to generate an output signal locked in frequency and phase to a reference signal, comprising:

a phase difference detector adapted to detect a phase difference between the reference signal and a signal derived from the output signal, the phase difference detector including:

a first bistable element clocked by the reference signal and having an output terminal to provide a first output signal;

a second bistable element clocked by the derived signal and having an output terminal to provide a second output signal;

a circuit block responsive to said first and second output signals to determine a change of a phase difference signal that is indicative of a phase difference between the reference signal and the derived signal;

a reset circuit having first and second input terminals respectively connected to receive said first and second output signals and adapted to determine a resetting of the first and the second bistable elements responsive to an attainment of a respective prescribed state of the first and the second output signals, said first and second input terminals of the reset circuit substantially symmetrical to each other from a point of view of a respective input impedance associated with each of them; and

a symmetrization element coupled to the output terminals of the first and second bistable elements, the symmetrization element including two transistors in a same circuit branch and having control terminals coupled to the respective output terminals of the first and second bistable elements; and

an oscillator controlled by the phase difference signal generated by the phase difference detector.

9. (Currently Amended) A method for improving linearity characteristics of a response of a phase difference detector adapted to generate a signal indicative of a phase difference between a first signal and a second signal, the phase detector having a first bistable element clocked by the first signal and having a first output signal, a second bistable element clocked by the second signal and having a second output signal, a circuit block to determine a variation of said signal indicative of the phase difference, responsive to said first and second output signals, a reset circuit having a first and a second inputs respectively connected to receive the said first and second output signals and adapted to determine a resetting of the first and second bistable elements in response to an attainment of a respective prescribed state by the first and the second output signals, and a symmetrization element coupled to the first and second bistable elements, the symmetrization element including two transistors in a same circuit branch and coupled to the first and second bistable elements, the method comprising:

making said first and second inputs of the reset circuit substantially symmetrical to each other from a point of view of an input impedance associated to each one of them by using the symmetrization element having the two transistors in the same circuit branch.

10. (Canceled)

11. (Previously Presented) The circuit according to claim 15 wherein the feedback circuit includes a delay circuit that provides a timed delay to the control input terminals of the first and second logic elements.

12. (Previously Presented) The circuit according to claim 15 wherein at least one of the control input terminals is a feed back terminal.

13. (Canceled)

14. (Canceled)

15. (Currently Amended) A phase difference detector, comprising:

a first logic element having an input terminal coupled to receive a first clock signal and having an output terminal;

a second logic element having an input terminal coupled to receive a second clock signal and having an output terminal;

a feedback circuit having two input terminals and an output terminal, a first input terminal being coupled to the output terminal of the first logic element and a second input terminal being coupled to the output terminal of the second logic element, the feedback circuit further including a logic gate coupled to the first and second output terminals from the first and second logic elements;

a feedback line coupled from the output terminal of the feedback circuit to a control input terminal in each of the first and second logic elements;

a phase correction circuit coupled to the output terminal of the first logic element and to the output terminal of the second logic element, the phase correction circuit having an output terminal to provide a phase correction signal; and

a symmetrization element coupled to the output terminals of the first and second logic elements, wherein the symmetrization element includes two transistors coupled in series

and having control terminals coupled to the respective output terminals of the first and second logic elements.

16. (Currently Amended) A phase difference detector apparatus, comprising:

a first element having an input terminal coupled to receive a first clock signal and having an output terminal and a control input terminal;

a second element having an input terminal coupled to receive a second clock signal and having an output terminal and a control input terminal;

a feedback circuit having two input terminals and an output terminal, a first input terminal being coupled to the output terminal of the first element and a second input terminal being coupled to the output terminal of the second element, the output terminal of the feedback circuit being coupled to a control input terminal in each of the first and second elements;

a phase correction circuit coupled to the output terminal of the first element and to the output terminal of the second element, the phase correction circuit having an output terminal to provide a phase correction signal; and

a symmetrization element coupled to the output terminals of the first and second elements, the symmetrization element including two transistors in a same circuit branch and having control terminals coupled to the respective output terminals of the first and second elements.

17. (Previously Presented) The apparatus of claim 16, further comprising a delay circuit to provide a timed delay to the control input terminals of the first and second elements.

18. (Previously Presented) The apparatus of claim 16 wherein the first and second elements comprise flip-flop devices.

19. (Previously Presented) The apparatus of claim 16 wherein the feedback circuit includes a logic element having at least one input terminal coupled to an output terminal

of the symmetrization element and an output terminal coupled to the control input terminals of the first and second elements.

20. (Previously Presented) The apparatus of claim 16, further comprising phase-locked loop means included along with the phase difference detector apparatus for realizing a frequency synthesizer.

21. (Previously Presented) The phase-locked loop circuit of claim 5 wherein the first and second bistable elements comprise flip-flop devices.

22. (Previously Presented) The frequency synthesizer circuit of claim 8 wherein the first and second bistable elements comprise flip-flop devices.

23. (Previously Presented) The frequency synthesizer circuit of claim 8, further comprising a delay device coupled to the symmetrization element to provide a delay to the first and second bistable elements.